Customer No.: 31561
Application No.: 10/709,307
Docket NO.: 12053-US-PA

AMENDMENT

In the Claims:

Claim 1. (currently amended) A double-triggered silicon controlling rectifier, comprising:

a P-type substrate;

a first N-well region, formed within the P-type substrate;

a second N-well region, formed within the P-type substrate, and on one side of the first N-well region;

a third N-well region, formed within the P-type substrate, and on another side of the first N-well region, opposite to the second N-well region;

a plurality of N+ diffusion areas, comprising:

a first N+ diffusion area, formed in the first N-well region and coupled to an external power terminal;

a second N+ diffusion area, formed in the first N-well region and on one side of the first N+ diffusion area, as a N-type trigger terminal of the double-triggered silicon controlling rectifier;

a third N+ diffusion area, formed in the first N-well region and on another side of the first N+ diffusion area, opposite to the second N+ diffusion area as the N-type trigger terminal of the double-triggered silicon controlling rectifier;

a fourth N+ diffusion area, partially formed in the third N-well region and partially formed in the P-type substrate, and on one side of the second N+ diffusion region,

opposite to the first N+ diffusion region as a cathode of the double-triggered silicon controlling rectifier; and

a fifth N+ diffusion, partially formed in the ~~third~~ second N-well region and partially formed in the P-type substrate, and on one side of the third N+ diffusion region, opposite to the first N+ diffusion region as the cathode of the double-triggered silicon controlling rectifier;

a plurality of P+ diffusion areas, comprising:

a first P+ diffusion area, formed within the first N-well region and between the first N+ diffusion area and the second N+ diffusion area, as an anode of the double-triggered silicon controlling rectifier;

a second P+ diffusion area, formed within the first N-well region and between the first N+ diffusion area and the third N+ diffusion area, as the anode of the double-triggered silicon controlling rectifier;

a third P+ diffusion area, formed within the P-type substrate between the first and the third N-well regions, and between the second and the fourth N+ diffusion areas, as a P-type trigger terminal of the double-triggered silicon controlling rectifier;

a fourth P+ diffusion area, formed within the P-type substrate between the first and the second N-well regions, and between the third and the fifth N+ diffusion areas, as the P-type trigger terminal of the double-triggered silicon controlling rectifier;

a fifth P+ diffusion area, formed within the P-type substrate and on one side of the fourth N+ diffusion area, opposite to the third P+ diffusion area, as a ground terminal of the double-triggered silicon controlling rectifier; and

a sixth P+ diffusion area, formed within the P-type substrate and on one side of the fifth N+ diffusion area, opposite to the fourth P+ diffusion area, as the ground terminal of the double-triggered silicon controlling rectifier; and

a plurality of isolation structures, formed within the P-type substrate and between spaces of the pluralities of N+ and P+ diffusion areas.

Claim 2. (original) The double-triggered silicon controlling rectifier of claim 1, wherein the isolation structures comprise shallow trench isolation structures.

Claim 3. (original) The double-triggered silicon controlling rectifier of claim 2, wherein a depth of the shallow trench isolation structure is about 0.4 μm for a 0.25-μm complementary metal-oxide-semiconductor (CMOS) process.

Claim 4. (original) The double-triggered silicon controlling rectifier of claim 1, wherein a portion of the isolation structures comprise dummy gate terminals.

Claim 5. (original) The double-triggered silicon controlling rectifier of claim 4, wherein the dummy gate terminal is made from polycrystal material.

Claim 6. (original) The double-triggered silicon controlling rectifier of claim 1, depths of the N+ and P+ diffusion areas are about 0.18 μm for a 0.25-μm complementary metal-oxide-semiconductor (CMOS).

Claim 7 (cancelled)

Claim 8 (cancelled)

Claim 9 (cancelled)

Claim 10 (cancelled)

Claim 11 (cancelled)

Claim 12 (cancelled)

Claim 13 (cancelled)